A Self-Checking Logic Cell

Sergey Tyurin, Alex Gorodilov

***Abstract*—** In the article a self-checked logic cell (SCLC) FPGA is proposed. Self-checking is performed by using the second half of the transmitting transistors tree, which verifies the active half. Additional transistors are needed to transmit settings to the active sub tree and to compare the results of calculations. The device is protected by a patent of the Russian Federation.

***Keywords*—** FPGA; Logic Cell; Look Up Table – LUT; Transmitting Transistors Tree.

I. INTRODUCTION

A field-programmable gate array (FPGA) consists of an array of logic blocks (Configurable Logic Block, CLB) [1]-[6], including of a few logical elements or cells (LE, LC). A typical logical cell consists of a 4-input LUT (Look Up Table), which is based on the tree of the transmitting MOS transistors – Fig.1:

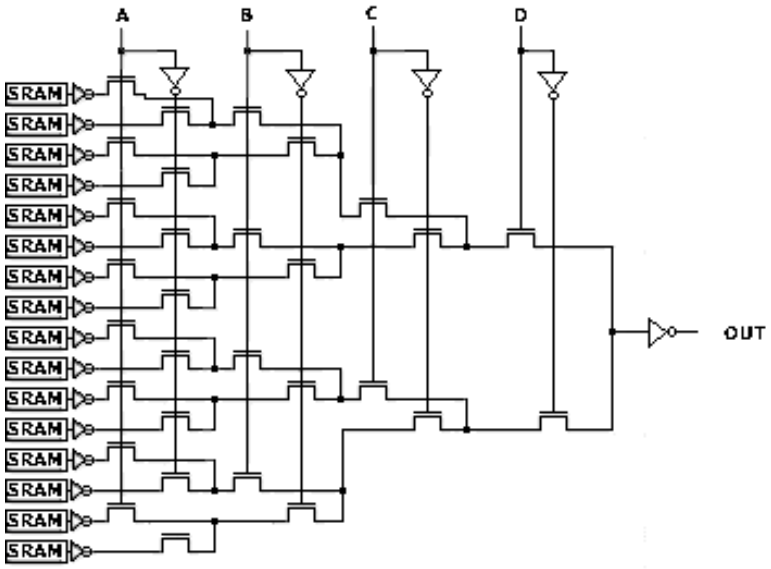

Fig.1 – Logic cell - a 4-input LUT FPGA

The truth table of the required logical function, for example F(ABCD), is loaded in the SRAM cells. They are usually uses LUT on 4,5 variables, they already adapt LUT to 6 and even on 7 variables, containing a large number of transistors. Therefore, validation of their functioning is actual. While calculating of the assigned logical function, one of the 2^n chains from the entrance to the output is activated in the tree of the transmitting transistors LUT. Studies in the region of highly reliable FPGA for the critical applications were activated recently. One of the leading experts in the field of PLD FPGA development Yervant Zorian thinks: "Now the main problem of system on a chip repair is development of embedded technologies and methods of the logic repair that occupies no more than 10% of chip area" [7]. It is most important with Radiation Hardened By Design (RHBD) in military and aerospace applications [4].

S. Tyurin, Perm National Research Polytechnic University, Perm, Russia (e-mail: tyurinsergfeo@yandex.ru).
A. Gorodilov, Perm State University, Perm, Russia (e-mail: gora830@yandex.ru).

II. A SELF-CHECKING

Self-checking is performed by using the second-half of the transmitting transistors tree, which verifies the active half. The comparison of the results of calculations is produced by element XOR (LUT-2) – Fig.2.

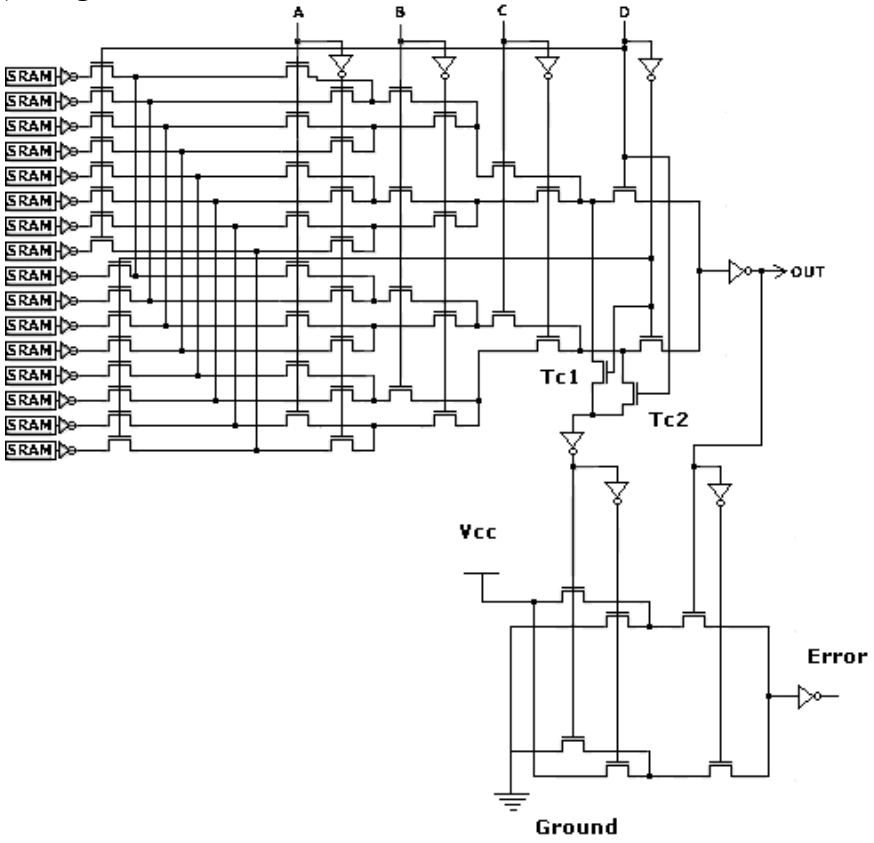

Fig.2 The self-checked logic cell SCLC

The redundancy of the tree of the transmitting transistors of SCLC with respect to LUT is evaluated by the expression:

$$\delta_{\text{C-LUTn}} = \frac{2^{n+1} + 2 \cdot n + 2^n + 16}{2^{n+1} + 2 \cdot n}. \quad (1)$$

We will obtain taking into account the memory of tuning:

$$\delta_{\text{SRAM+C-LUTn}} = \frac{2^{n+1} + 2 \cdot n + 2^n + 16 + 8 \cdot 2^n}{2^{n+1} + 2 \cdot n + 8 \cdot 2^n}. \quad (2)$$

The graph of change (2), constructed in system “MathCAD” is represented in Fig.3.

Thus, with n=4 we obtain the redundancy of order 17%. With an increase in n the redundancy approaches 10%!

The authenticity of the SCLC (P) functioning can be evaluated by the expression:

$$P_{\text{D-C-LUTn}}(t) = e^{-\cdot(2^{n+1}+2n+2^n+16)\lambda \cdot t} + 2 \cdot (1 - e^{-\cdot(\frac{2^{n+1}+2^n}{2})\lambda \cdot t}) e^{-(\frac{2^{n+1}+2^n}{2})\lambda \cdot t} \cdot e^{-(16+2n)\lambda \cdot t}. \quad (3)$$

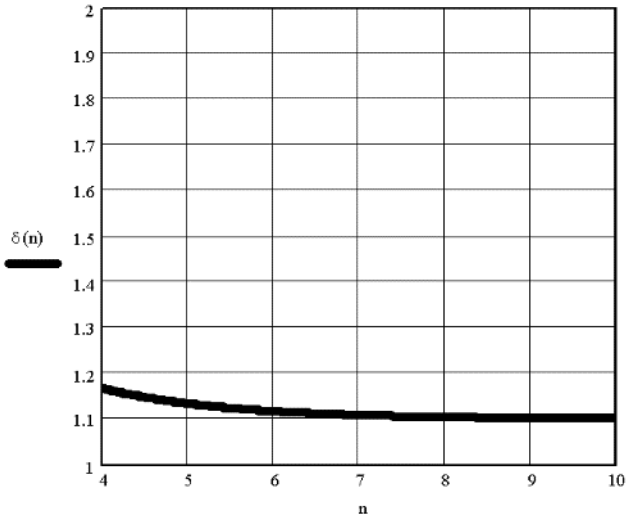

Fig.3.The graph of the redundancy change

The authenticity of the functioning of the tree LUT:

$$P_{1\text{-}LUTn}(t) = e^{-(2^{n+1}+2n)\lambda \cdot t} \quad (4)$$

Comparison of the authenticity of the functioning of the tree LUT (4) and SCLC (3) for $\lambda=10^{-8}$ are described in Fig.4.

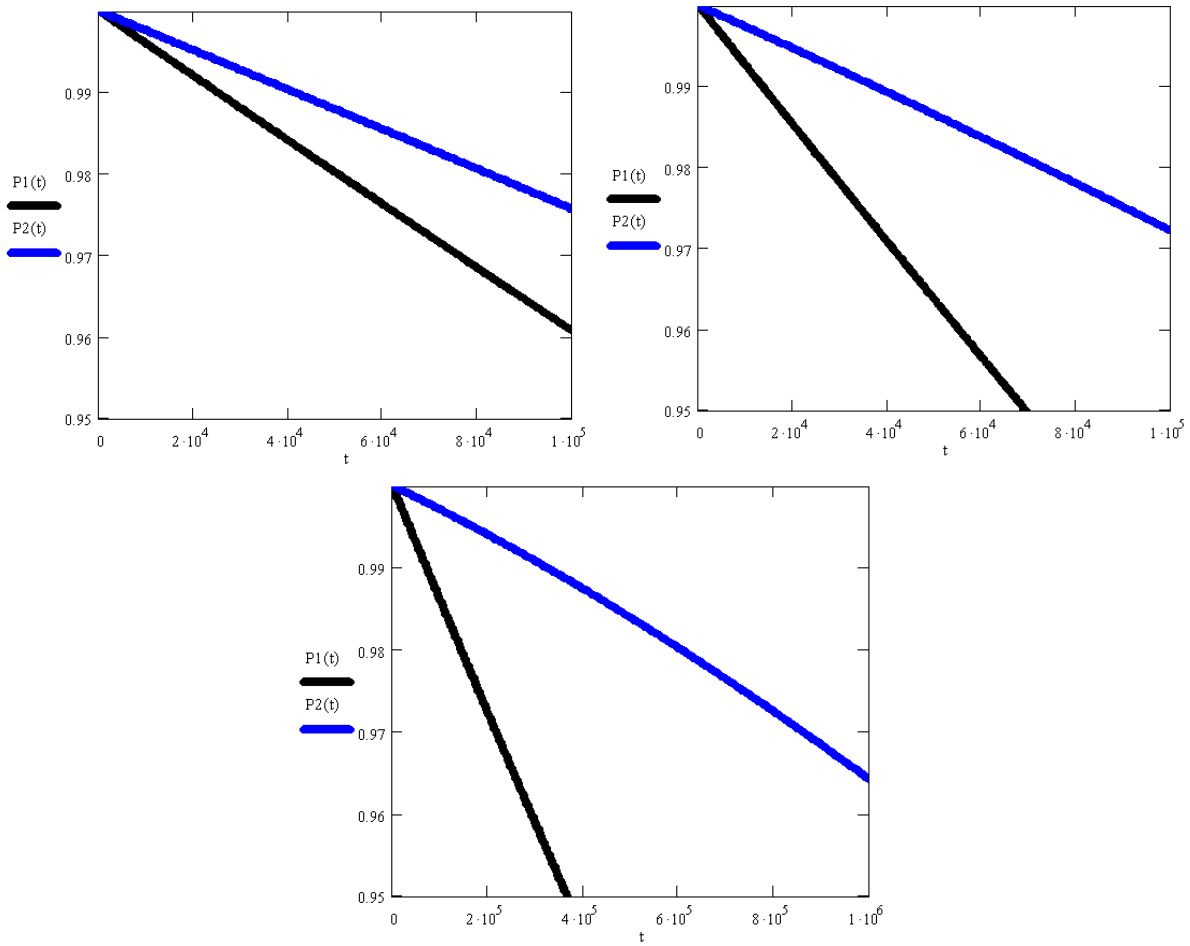

Fig.4 Comparison of the authenticity of the functioning of the tree LUT and SCLC for n=4, n=5 and n=6.

Thus, we obtain significant gain in the authenticity of the functioning.

III. SIMULATION OF THE SCLC

Simulation was carried out in the system NI Multisim 10 by National Instruments Electronics Workbench Group [8]. Model of the SCLC-2 is presented in Fig. 5.

Implementing XOR element based on LUT-2 is presented in Fig. 6:

The modeling disconnection d0-d2 transmission 1 to d2. At the output of XOR observe the error signal (Fig. 7). In case of transfer of 0 to d2-error signal is not generated (Fig. 7)

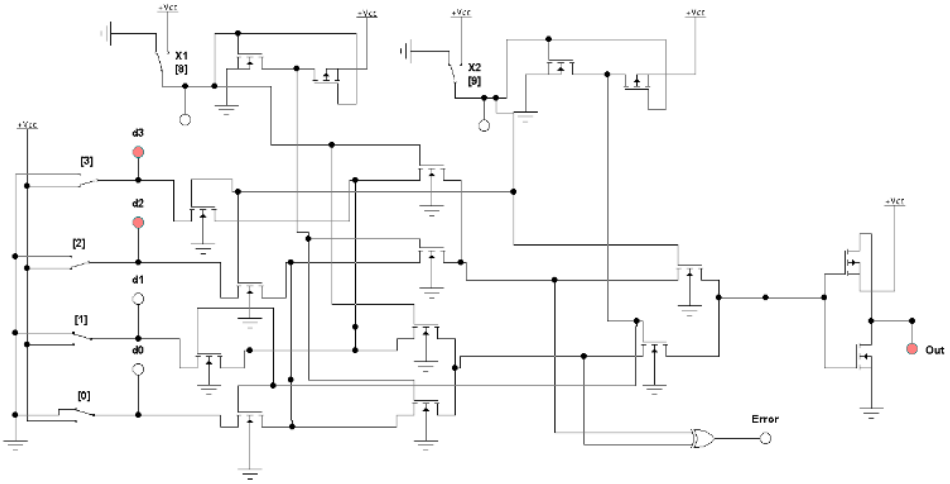

Fig. 5. Model of the SCLC-2 in the system NI Multisim 10. Transfer with zero input 0.

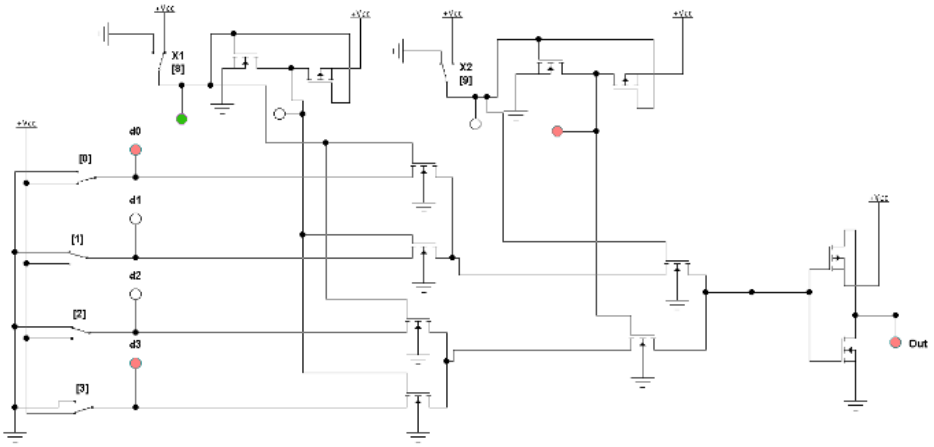

Fig. 6. Implementing XOR element based on LUT-2(x1=1, x2=0).

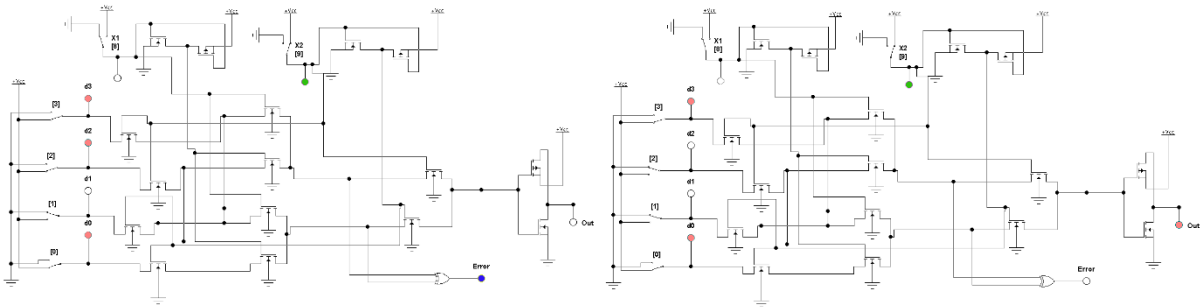

Fig. 7. The modeling disconnection d0-d2 transmission 1 to d2 and 0 to d2.

So break will be fixed only by transferring 1. Accordingly, the circuit connection to the bus «Ground» or permanently closed transistor is detected during transmission 1.

IV. CONCLUSION

The proposed self-test logic cell can detect the problem and accelerates the recovery of FPGA logic. Analysis shows that the authenticity of checking tree LUT in a number of cases proposed can exceed the authenticity of duplicating. The simulation SCLC in the system NI Multisim 10 confirms the performance of the proposed scheme. To ensure reliable setup (SRAM) and inverter input variables, such as the use of methods [9], [10]. Further studies taking into account proposed in the article approaches are expedient. The device is protected by a patent of the Russian Federation [11].

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