Advanced logic cell FPGA

Ruslan Vikhorev, Sergey Tyurin

***Abstract*—** Look-up table (LUT) realizing system from m of logic functions – DC-LUT is presented in this paper. The structure of the disjunctions block of constituents is improved considering the requirement that only one diagram way shall be activated. The carried out modelling in the circuit design system NI Multisim 10 by National Instruments Electronics Workbench Group confirms the operability of the proposed improved technical decision for the disjunctions block of DC–LUT constituents.

***Keywords*—** Boolean functions, FPGA, PDNF, Look-up table (LUT).

I. Introduction

FPGA PLD Logic Cell, often called LUT (Look Up Table – truth table), is based on a multiplexer that represents a tree of elementary multiplexers 2-1 on the basis of the transmitting MOS transistors, the input of which are configured by the so-called reconfigurable cells of static memory SRAM [1]. Any functions, including constants, may be implemented by uploading the truth tables values of n variables functions into a configuration memory SRAM.

A typical cell consists of a 4-input LUT (RAM address inputs), but the modern up-to-date FPGAs have the complicated, configurable 6,7-input LUTs. There are reports that the 8-input LUTs exist [4].

II. DC-LUT logic element

As known, the drains and sources of the CMIS transistors used in LUT with the same topological characteristics are actually equivalent. A transistor circuit, inverse to the LUT structure, can be created by “making a U-turn” [5,6] - Fig.1.

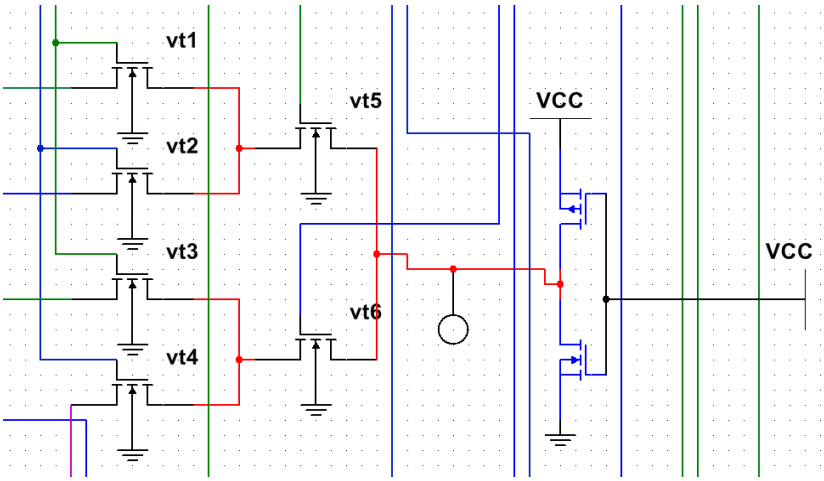

Fig. 1 Transistor circuit – DC –LUT 2 decoder.

By doing so, in accordance with design rules for the circuits from the transmitting transistors, an alternative line should be created for each output invertor to convert its output into “1’.

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Therefore, a dual to conjunction expression describing the corresponding line in the inverse tree should be used – Fig.2.

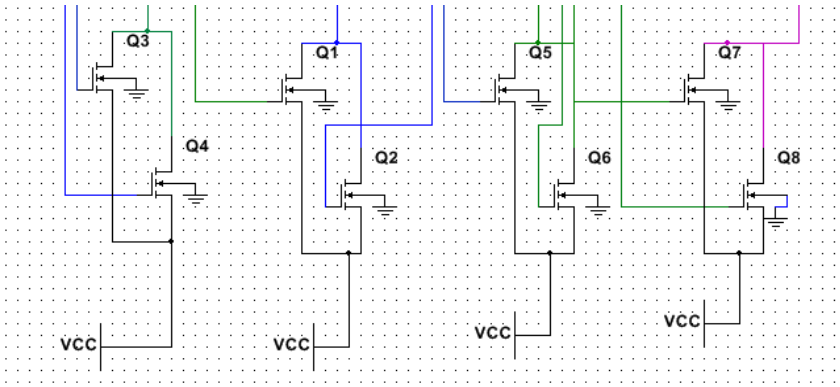

Fig. 2 DC LUT2 zero bit with alternative line.

We got a decoder with z output functions as follows (without regard to alternative lines):

$$\bar{z}_i = \&x_j^{\sigma_j^{2^n}}, i = 0...2^n - 1, j = 1...n.$$

Then, by uniting the corresponding outputs from 2^n ones by "OR" [5,6], we implement the n-digit logic functions system on the basis of the principal disjunctive normal forms (PDNF).

The connections of the outputs 0,1,2,2 can be programmed with the corresponding OR elements in order to implement the logic functions systems. It can be programmed similarly to the interconnects programming [1] - Fig.3. Thus, the disjunctions blocks of the logic functions constituents may be implemented in a manner shown in Fig.3.

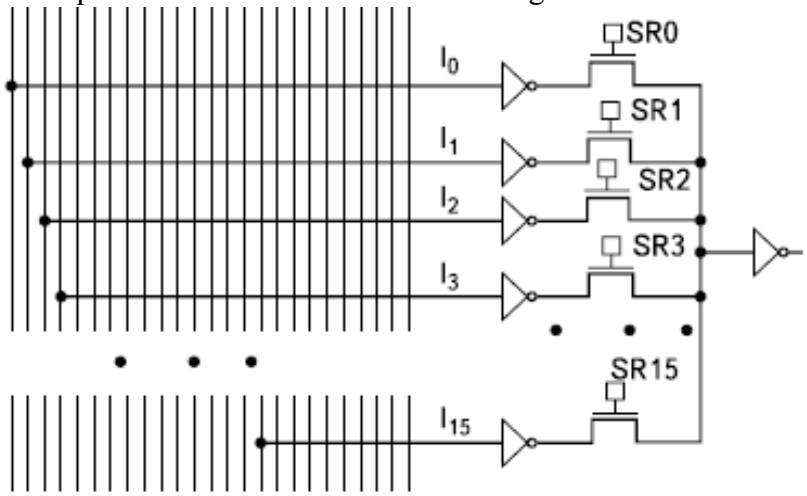

Fig. 3 Programmed interconnects for 16 directions (SR0…15 configuration memory SRAM).

III. IMPROVING DISJUNCTIONS BLOCK CONFIGURATION METHOD

The former suggested disjunctions block of the logic function constituents [5,6] have looked as shown in Fig.4.

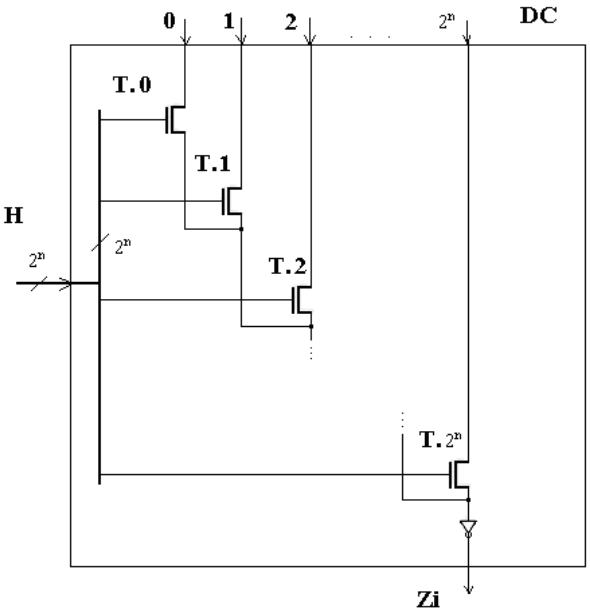

Fig. 4 Initial implementation of disjunctions block of the logic function constituents.

It has been supposed that configuration H for implementing required disjunction of constituents from the modified tree of DC transistors was carried out with the help of the configuration memory [1,8,9,10], not shown in Fig.5. However such implementation does not meet the requirements [7], because more than one MOS transistor can be activated simultaneously – the configuration arrives at gates, whereas the signals from the modified tree of DC transistors arrive at the sources. That is why, the disjunctions block diagram should be changed and look like it shown in Fig.5.

In the diagram of Fig.5 the signals from the modified tree of DC transistors activate the only gate of the only MOS transistor.

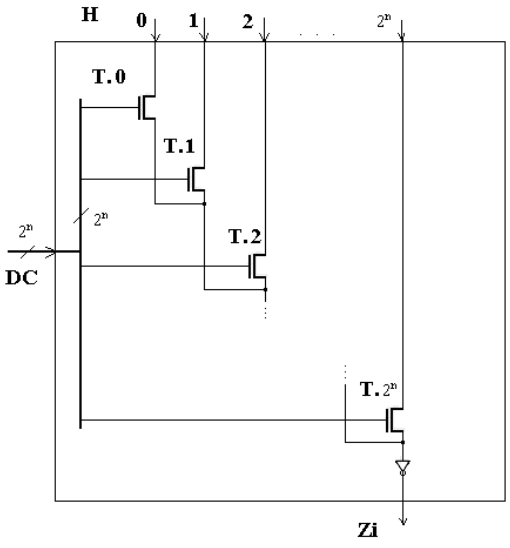

Fig. 5 Improved disjunctions block of the logic function constituents.

IV. Modelling logic element for implementing logic functions with improved disjunctions block of the logic function constituents

Let model a logic element for implementing logic functions with improved disjunctions block of the logic function constituents for n=2 (Fig.6) in the circuit design system NI Multisim 10 by National Instruments Electronics Workbench Group. In Fig.7 the keys X1, X2 model the

variables. In Fig. 8 The keys S1- S4 model the configuration H.

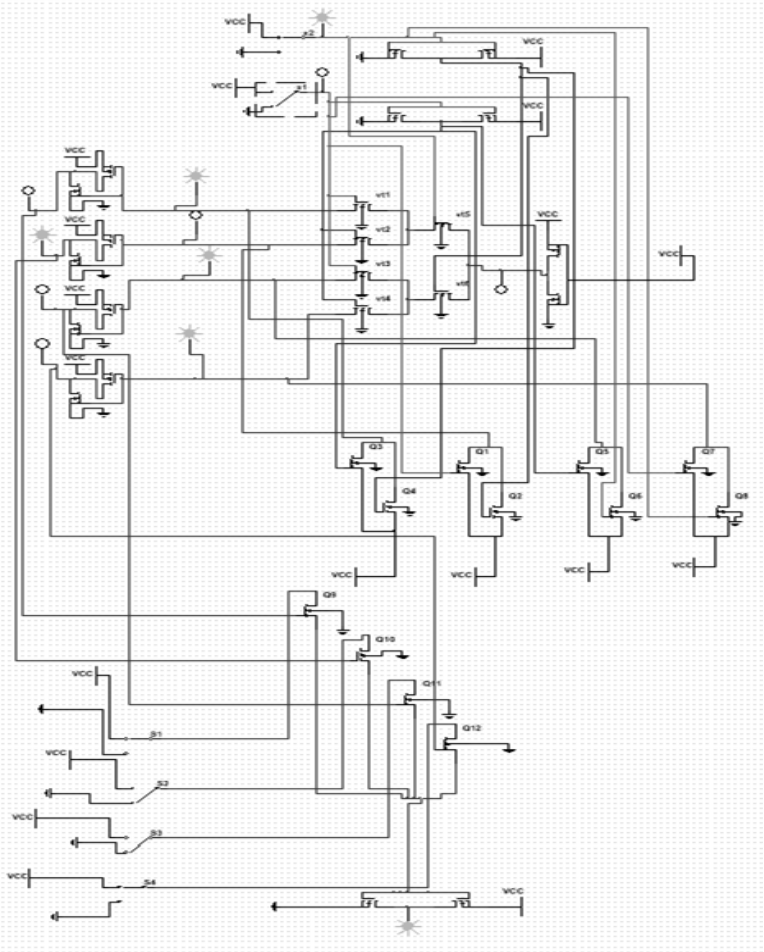

Fig. 6 Logic element for implementing logic functions with improved disjunctions block of the logic function constituents for n=2 with one improved disjunctions block of the logic function constituents.

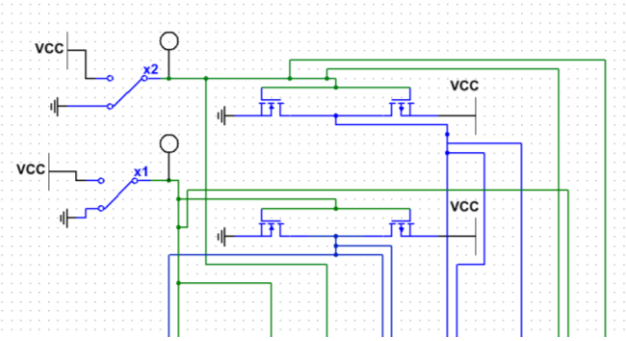

Fig. 7 The keys X1, X2.

The gates of disjunctions block transistors are controlled by invertors installed in the outputs of the detailed (regard to the standard LUT) transistors tree. At the same time, the alternative lines provide the transmission of the logic units when the tree is not activated. Fig.7 shows implementation of the function “Excluding OR” – a LED lights in the OR block output, because the variables X1,X2 have different values.

The carried out modelling confirms the operability of the proposed improved technical decision for the disjunctions block of DC–LUT constituents, an application for a patent is applied.

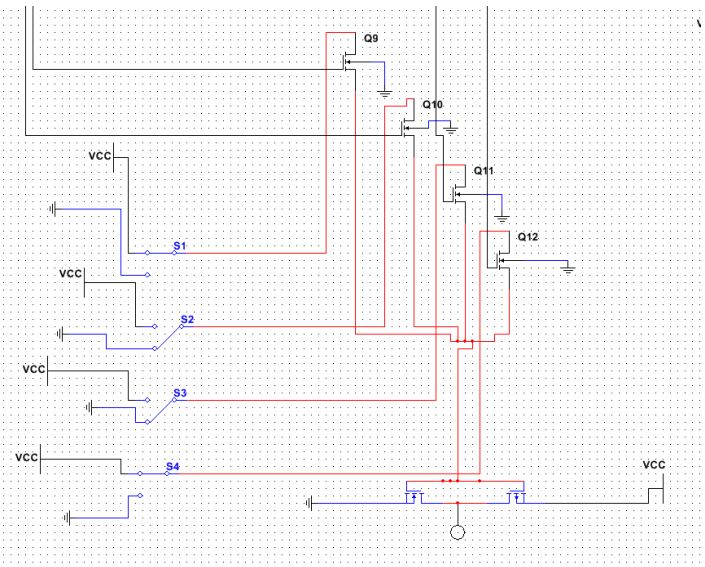

Fig. 8 One improved disjunctions block of the logic function constituents.

V. CONCLUSIONS

Thus, the structure of the proposed logic element of DC LUT decoder is modified for implementing the systems of the functions in the FPGA PLD, which is based on the diagram of the MOS transistors tree. The structure of the disjunctions block of constituents is improved considering the requirement that only one diagram way shall be activated.

In the changed diagram, the signals from the modified tree of DC transistors arrive at the gates of the disjunctions block MOS transistor, whereas the configuration data from the configuration memory arrives at the sources of these transistors.

The carried out modelling in the circuit design system NI Multisim 10 by National Instruments Electronics Workbench Group confirms the operability of the proposed improved technical decision for the disjunctions block of DC–LUT constituents.

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